Real-Time Embedded System Support for the BTeV Level 1 Muon Trigger

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Abstract

The Level 1 Muon Trigger subsystem for BTeV will be implemented using the same architectural building blocks as the BTeV Level 1 Pixel Trigger: pipelined field programmable gate arrays feeding a farm of dedicated processing elements. The muon trigger algorithm identifies candidate tracks, and is sensitive to the muon charge (sign); candidate dimuon events are identified by complementary charge track-pairs. To ensure that the trigger is operating effectively, the trigger development team is actively collaborating in an independent research program for reliable, self-aware, fault-adaptive behavior in real-time embedded systems (RTES). Key elements of the architecture, algorithm, performance, and engineered reliability are presented.

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Summary

In an effort to reduce cost and improve system reliability, the Level 1 Muon Trigger for the BTeV experiment at Fermilab is being designed to employ similar, if not identical, hardware elements of the Level 1 Pixel Trigger [1, 2]. In particular, data from the muon detector will arrive on optical links, be reformatted and sorted by field programmable gate arrays (FPGAs), and processed by a farm of dedicated computational elements. For the baseline architecture the processor farm consists of approximately 250 Texas Instruments TMS320C64xx digital signal processors (DSPs), each delivering in excess of 3×10^9 instructions per second. The Pixel Trigger farm will be constructed from the same modules, and be an order of magnitude larger. The Muon Trigger algorithm examines data from each octant of the detector, and separately searches each of the views (radial, and U/V stereo) in 3 stations of each octant to find tracks originating from the proton-antiproton beam interaction point. The algorithm also estimates the sign of the curvature for each track. Track pairs with complementary sign indicate the likelihood of a dimuon event. Monte Carlo studies of the trigger efficiency and rejection show that the architecture will meet the requirements of BTeV, and timing studies using similar albeit slower (TMS320C6711) DSPs indicate that the number of processors should be sufficient to keep up with the anticipated data rate.

There will be hundreds of independently operating elements (FPGAs and DSPs) in the Muon Trigger, and thousands in the Pixel Trigger. Commissioning and reliability are serious concerns. To address these concerns, an independent research project funded by the NSF has undertaken the study of self-aware and fault-adaptive real time embedded systems (RTES [3]), for which the BTeV Trigger will serve as a proving ground. The RTES project is a multi-university collaboration consisting primarily of computer science and electrical engineering researchers in the area of reliable systems. The project is developing very lightweight agents (VLAs) for monitoring and corrective action on the dedicated processing elements, and adaptive reconfigurable mobile objects for reliability (ARMORs) to provide systematic assurance that critical processes are running correctly.

A brief overview of the experiment, followed by details of the trigger architecture and its performance are presented. This includes both physics efficiency and rejection, as well as actual processing time under differing loads using the C6711 DSP for the Muon Trigger code. Further, the effects of interaction between the Muon Trigger development and the RTES project are reported. For example, the Muon Trigger code has been used as the basis for characterizing the OS/kernel features required by the physics application: hardware and software interrupt service, with preemptive scheduling of prioritized tasks, etc. Also, the algorithm has served as a test case for understanding minimal impact software instrumentation, such as TI's real time data

exchange (RTDX). RTDX employs otherwise unutilized JTAG resources for real time communications. In addition, the approach of FPGA-based monitoring of the trigger execution, using key-coded watch-dog timers is reported.

References

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